(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: 0 276 068 B1

(12) # EUROPEAN PATENT SPECIFICATION

(45) Date of publication of patent specification: 05.04.95 Bulletin 95/14

(51) Int. Cl.[6]: G06F 15/80

(21) Application number: 88300202.4

(22) Date of filing: 12.01.88

(54) **An associative computation network.**

(30) Priority: 20.01.87 US 5248

(43) Date of publication of application: 27.07.88 Bulletin 88/30

(45) Publication of the grant of the patent: 05.04.95 Bulletin 95/14

(84) Designated Contracting States: DE FR GB

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Description

Electronic neural networks have been described by J. J. Hopfield in "Neurons With Graded Response Have Collective Computational Properties Like Those of Two-state Neurons", *Proc. Natl. Sci., USA* Vol. 81, pp. 3088-3092; and by J.J. Hopfield and D. W. Tank in "'Neural' Computation of Decisions in Optimization Problems", *Biological Cybernetics*, Vol. 52, (1985), pp. 141-152; as well as in U. S. patent application Serial No. 693,479 filed on behalf of J. J. Hopfield on January 2, 1985; and U.S. patent application Serial No. 795,789 filed on behalf of J. J. Hopfield and D. W. Tank on November 7, 1985.

Basically, the Hopfield neural network described in the above references is a highly parallel computational circuit comprising a plurality of amplifiers, with each of the amplifiers feeding back its output signal to itself and all of the other amplifiers through conductance T_{ij}. The T_{ij} conductances (where T_{ij} denotes the conductance between the output of amplifier j and the input of amplifier i) and the associated connections can be thought of as comprising a feedback network which has one output signal set and two input signal sets. The output signal set is applied to the amplifier inputs, one of the input signal sets is derived from the amplifier outputs, and the other input signal set is responsive to input stimuli applied to the neural network. As shown in the prior art, one can explicitly specify the values of the T_{ij} conductances to achieve predetermined results, such as reaching different specified output states of the amplifier in response to different ranges of input stimuli. Also as described in the prior art, an input interconnection network may be interposed between the input stimuli and the second set of inputs of the feedback network. The input interconnection network permits manipulation of the expected input signals to corresponding signals that drive the feedback network and the amplifiers.

The neural network model described most extensively in the prior art is one with symmetric couplings, i.e., the connections between pairs of neurons satisfy the relationship $T_{ij}=T_{ji}$. The dynamics of such a network is relatively simple. The system moves in the direction of reducing a global energy function of the circuit, E, to states that are local minima of E, and once a local minimum is reached, the circuit remains at the stable state until perturbed by a sufficiently large input signal that moves the circuit to a different local minimum. The local minima may be thought of as the stored "memories" that are characterized by the vectors M^v. An associative memory can be constructed with the Hopfield neural network by constructing the connection strengths T_{ij} in accordance with the outer product, or Hebb, rule; to wit, by assiging

$$T_{ij}=\sum_{v=1}^{n} M_i^v M_j^v$$

for j≠i, and 0 otherwise. In a very simple embodiment T_{ij} = -1 (an inhibitory connection) for i≠j and 0 otherwise, resulting in a network that behaves as an n-flop; that is, a multi-output version of the well-known, two-output network commonly known as a flip-flop.

The Hopfield neural network is a very robust network, in the sense that it is able to associatively recall the stored memories even when the input is heavily distorted by noise, or when some of the hardware connections are inoperative. On the other hand, the Hopfield network must be sparsely populated with stored information, and some work has been done which indicates that the number of stored vectors in a Hopfield network should be limited to approximately 0.15N, where N is the number of amplifiers. Also, computation of the T_{ij} values in the Hopfield network (for the general case) is not easy, and the precise location of the boundaries between regions of attraction of the memories is not easily controlled.

According to this invention there is provided a network as claimed in claim 1.

Advantages of embodiments of the invention include a network structure that allows for simple and efficient programming of the memories into the network, and an arrangement that can easily be implemented in integrated circuit technology.

An associative computation network embodying the invention that is capable of storing K vectors of N bits each includes a decision network (e.g., a K-flop network) and a feedback arrangement that, functionally, is separable into two serially connected networks. The first network has its inputs connected to the outputs of the decision network and is arranged to develope K sets of excitatory and inhibitory drive signals. Each set corresponds to a stored vector and, more specifically, each "1" in the stored vector gives rise to an excitatory drive signal while each "0" gives rise to an inhibitory drive signal. For each different output state of the decision network, a different one of the K sets appears at the output of the first network. The output leads of the first network, which may also be employed as the input interface leads to the associative computation neural network, are connected to the second network. The second network develops K output signals that are applied to inputs of the decision network. The output signals of the second network are proportional to the projection of the input signals applied to the second network on the stored vectors. In one embodiment, the projection is obtained with connections in the second network that are excitatory when the applied input is excitatory and the corresponding component in the stored vector is a "1", and non-excitatory otherwise. This corresponds to an AND function of the inputs signals to the

second network with the stored vectors. In another embodiment, the projection is obtained with an Exclusive NOR projection of the inputs signals to the second network with the stored vectors. In still another embodiment there is included another set of amplifiers that is interposed between the output of the first network and the input of the second network. A correlative application is also described.

Brief Description of the Drawing

FIG. 1 presents a schematic diagram of my associative computation network;

FIG. 2 shows an efficient realization of the decision network in FIG 1;

FIGS. 3 and 4 illustrate one realization for implementing the C_{ij} and C'_{ij} connections of the FIG. 1 networks;

FIG. 5 depicts a physically rearranged structure of my FIG. 1 network that interleaves networks 20 and 40 and thereby permits the use of a single memory cell for each bit in the set of stored vectors to control both networks;.

FIG. 6 illustrates a different schematic diagram of my associative computation network;

FIG. 7 presents a correlator application of my associative computation network; and

FIG. 8 illustrates the various storage arrangements and output ports of the FIG. 1 network that may be useful in different applications.

Detailed Description

FIG. 1 presents a diagram of one embodiment of the invention. It comprises a vector units network 10, a template projection network 20, a decision network 30, and a template generator network 40; all interconnected in a feedback loop. A careful perusal of FIG. 1 would reveal that the demarcation lines between the various above-named segregated units is largely arbitrary, but it is convenient to choose some borders so that a functional description of the circuit is made easier. Indeed, as shown infra, some of the segregated units may be coalesced to form more compact realizations of my invention.

Vector units network 10 in FIG. 1 serves as the gateway into which input signals are injected via lines 12 and from which the output signals are derived via lines 15. More specifically, network 10 comprises N amplifiers 11, where N is the number of bits that each output vector is desired to have. Input signals are fed into the inputs of amplifiers 11, and the output signals of the FIG. 1 network are obtained from the output signals of amplifiers 11. In addition to contributing to the outputs of the FIG. 1 neural network, the outputs of amplifiers 11 are fed to template projection network 20. Network 20 comprises N input leads and K output leads, where K is the number of stored "memories", or stable states, of the FIG. 1 network. These stable states form a set of the desired output vectors (each being N bits long). The input and output leads of network 20 form a grid, and the junction points of the grid comprise interconnection nodes which, for convenience, are designated C_{ij}, where i marks the output lead and j marks the input lead of network 20. With this arrangement, the i^{th} output line of network 20 drives the subsequent network (network 30) with a signal that is related to

$$\sum_{j=1}^{K} A_j C_{ij},$$

where A is the output voltage of the j^{th} amplifier 11.

The collection of interconnection nodes for each of the K output leads of network 20 is related to a stored vector. That is, each stored vector M_i is defined by bits $M_{i1}, M_{i2}, \ldots M_{ij}, \ldots M_{iN}$ and is embodied, in a sense, in $C_{i1}, C_{i2}, \ldots C_{ij}, \ldots C_{iN}$. The correspondence between each C_{ij} and M_{ij} (i.e., the manner imparting the M_{ij} information to the connection) relates to the metric that is selected, as described in greater detail below. Basically, however, the C_{ij} connections develop a a measure of how closely the input signals reflect the expected output vector. Stated even more generally, any arrangement of C_{ij} is acceptable as long as the output signals of network 20 provide a measure by which the projection of the input signals on the stored vectors can be ascertained. Typically, that means that the C_{ij} connections are such that when network 10 resides at a state which corresponds to one of the stored vectors, network 20 develops output signals where one and only one of the output lines of network 20 provides a maximum drive to network 30.

As an example of C_{ij} connections, when the stored vectors are such that no stored vector subsumes any other stored vector, then the C_{ij} connections can be selected to be excitatory when the j^{th} bit of the stored vector is a "1" and non-excitatory when the j^{th} bit of the stored vector is a "0". (An excitatory connection is one that tends to turn a subsequent amplifier "on", a non-excitatory connection is one that has no effect on a subsequent amplifier, and an inhibitory connection is one that tends to turn a subsequent amplifier "off." Sometimes there is no practical difference between a non-excitatory connection and an inhibitory connection.) Thus, with a set of stored vectors that do not subsume each other, the connections C_{ij} can correspond to

$$C_{ij} = \mathrm{AND}(V_j, M_{ij}),$$

where AND stands for the logical AND function, and V_j takes on the logic value "1" when the j^{th} amplifier 11 is "on" and logic "0" otherwise.

In applications where the above limitation on the stored vectors is not acceptable, the character of the connections can, for example, be selected to follow

the equation

$$C_{ij} = \mathrm{EXNOR}(V_j, M_{ij}),$$

where EXNOR is the logical Exclusive NOR function. Other metrics are, of course, also possible.

It should be noted, perhaps, that the above two metrics are different from the one used in the prior art neural network feedback loop, where the algebraic product ($T_{ij}U_j$) is employed and where the T_{ij} values are multiplicative constants. The above metrics, on the other hand, utilize logical relationships. It should not be viewed, however, that my invention is limited to logical relationships. To the contrary, the above examples aim to show that the connections in my invention can have algebraic, logical, or any other useful functional relation to the stored vectors.

As indicated above, the output leads of template projection network 20 are connected to decision network 30. The function of network 30 is to respond to the projection signals developed by network 20 and develop therefrom the drive signals for network 40 that would place network 10 in a state that corresponds to the one vector stored in network 40 that is closest to the input signals appearing at network 20.

In many applications the function of network 30 comes down to selecting the output line of network 20 with the largest driving function and turning "on" a corresponding output line of network 30 while turning "off" all other output lines of network 30. That is, in such applications the input to network 30 is a set of K signals, with one input signal (e.g., p^{th}) being the largest. The output of network 30 is also a set of K signals, E_1, E_2, ... E_K, with one output signal (e.g., E_p) being high, or "on," and all other output signals being "off". This mutually inhibiting type of network 30 is achieved in the FIG. 1 network with a simple K-flop Hopfield network (described above) of K amplifiers 31 and a local feedback network 32, where the T_{ij} connection coefficients in feedback network 32 follow the relationship $T_{ij} = -1$ when $i \neq j$ and 0 otherwise. A different realization of a K-flop network is shown in FIG. 2 and described below.

The K-flop realization for network 30 is the simplest, but it certainly is not the only one. For example, a "largest" projection signal at the input to network 30 may be designed to turn "on" more than one output line of network 30, or designed to induce different analog signals at the outputs of network 30.

Turning attention again to FIG. 1, the output signals of network 30 are applied to template generator network 40. Structurally similar to network 20, template generator network 40 has K input leads and N output leads that internally form a grid. The junction points of the grid comprise interconnection nodes which, for convenience, are designated C'_{ij}, where i marks the i^{th} input lead and j marks the j^{th} output lead of network 40. Since network 40 is the template generator network, in applications where network 30 is a K-flop the connectivity is $C'_{ij} = M_{ij}$, where $C'_{ij}=1$ corresponds to an excitatory connection, and $C'_{ij}=0$ corresponds to an inhibitory connection. The output leads of network 40 are connected to the inputs of vector units network 10, and in this manner network 40 strives to maintain network 10 at a state that corresponds to one of the stored vectors.

Although a specific interconnection approach is described above for network 40 (C'_{ij}), it should be realized that any drive approach will do as long as the input lines to network 40 cause the delivery of a set of drive signals that tend to place network 10 at a state that corresponds to a stored vector. Of course, a K-flop input to network 40 does result in a very simple correspondence between the stored vectors and the C'_{ij} connections.

To assist in moving the network of FIG. 1 to a different state, network 30 includes a control lead 33 that turns "off" all of the amplifiers in network 30. When control 33 is activated, amplifiers 33 develop no output voltage, and that condition disables the inhibitory action of network 32 and the driving action of network 40 (driving the amplifiers of network 10). Input lines 12 are then employed to apply an appropriate voltage to each amplifier 11, placing network 10 in a different state. In accordance with the above described operation of network 20, the new state of network 10 develops a set of template projections onto the output lines of network 20. The output line of network 20 whose C_{ij} connections correspond to a stored vector that is closest (by the metric chosen) to the newly forced state of network 10 is now the one that injects the maximum current into network 30. As control 33 is deactivated, the input line with the largest injecting current is the first one to turn its corresponding amplifier "on", and that amplifier inhibits all other amplifiers via network 32 in accordance with the K-flop action of network 30. The output line of network 30 that is turned "on" causes template generator network 40 to appropriately apply excitatory and inhibitory signals to the various amplifiers in network 10, placing the network into the quiescent state corresponding to the vector that matches most closely (has largest projection value in accordance the metric chosen for network 20) to the state to which network 10 was initially placed by the applied input.

FIG. 2 presents an efficient realization of the K-flop decision network 30. In FIG. 2, amplifiers 31 are implemented in the form of three-input AND gates, where the output of each AND gate 31 is connected to a serial connection of two complementary MOS switches 34 and 35 that are connected between one of the AND gate inputs and ground. A second input of all AND gates 31 is connected to control line 33, and the remaining inputs of AND gates 31 form the inputs to network 30. Switches 34 and 35 in FIG. 2 are a p-channel switch 34 and an n-channel switch 35. Switch 34, connected to the AND gate's input, is open when its control voltage is high and closed when its control

voltage is low. Conversely, gate 35 is closed when its control voltage is high and open when its control voltage is low. The junction points of the complementary switches are all connected to a source V_{DD} via inhibit line 36 and a resistor. In operation, a low voltage on control lead 33 disables gates 31. Consequently, switches 34 are closed, switches 35 are open, and line 36 is high. As soon as control lead 33 goes high, gates 31 begin to turn "on" under the influence of the drive signals applied to network 30. The gate with the largest drive signal turns "on" first, and it reverses the states of the switches connected to it. The associated switch 35 drives line 36 to a low state and, through closed switches 34, the low level on line 36 causes all gates 31 to turn "off"; except the gate that turned "on" first, (because its associated switch 34 was opened by the turned "on" gate 31).

The C_{ij} and C'_{ij} connections of networks 20 and 40 can be implemented by physically affixing the M_{ij} bits of the stored vectors within the circuitry that realizes the C_{ij} and C'_{ij} connections within networks 20 and 40. It makes for a more versatile circuit, however, when the M_{ij} bits can be stored in networks 20 and 40 in an alterable way, such as within accessible memory cells.

FIG. 3 depicts one embodiment for developing the C_{ij} connections of network 20 through the use of memory cells. Line 15 is an input line of network 20 and line 21 is an output line of network 20. Block 22 is a cell, e.g., a flip-flop, which holds the value of M_{ij}. To obtain the EXNOR connectivity described above, the required logical function that must be developed is $V_j \cdot M_{ij} + \overline{V_j} \cdot \overline{M_{ij}}$. This logical function is realized in FIG. 3 with the arrangement of transistors 23, 24, 25 and 26. Transistor 24 is turned "on" by a true value on line 15 while transistor 23 is turned "on" by a true value at the output of cell 22. Transistors 23 and 24 are connected in serial fashion and interposed between a voltage source V_{DD} (to which resistor 27 is connected) and line 21. In parallel with the serial connection of transistors 23 and 24 is a serial connection of transistors 25 and 26. Transistors 25 and 26 are turned "on" by a false value at the output of cell 22 and on line 15, respectively.

FIG. 4 depicts one embodiment for developing the C'_{ij} connections of network 40. Line 12 is an output line of network 40 and line 41 is an input line of network 40. As in FIG. 3, block 22 is a cell which holds the value of M_{ij}, and that value is communicated to line 12 via transistor switch 43, under control of line 41.

Recognizing that C_{ij} and C'_{ij} are both controlled by cells 22 in the above-described embodiments, it is clear that VLSI implementation advantages can be had by combining networks 20 and 40. FIG. 5 illustrates one way for interleaving the input and output lines of networks 20 and 40 so that any cell 22 can easily control the necessary current flow. The input and output lines of amplifiers 11 form columns in FIG. 5, and the input and output lines of amplifiers 31 form rows in FIG. 5. The nodes where output column lines and input row lines intersect contain the C_{ij} connections, and the nodes where output row lines and input column lines intersect contain the C'_{ij} connections. For sake of clarity, FIG. 5 includes a blow-up of a portion in FIG. 5 that encompasses both a C and a C′ connection, illustrating the fact that a single M_{ij} cell controls both connections.

Although the connections to, and from, cells 22 are not shown in FIG. 5, it is easy to appreciate that the various cells storing the M_{ij} bits in the structure of FIG. 5 can be interconnected in a serial, shift register, fashion to permit loading of the M_{ij} values of the vectors to be stored from 1, N, or K ports, as desired; or arranged to be addressed as a conventional RAM.

The arrangement of FIG. 1 includes amplifier network 10, which provides regeneration and a degree of isolation between the shown input and output ports. In some applications, however, it may be desirable to do without amplifiers 11. This can be accomplished by replacing the current drive supplied by C'_{ij} with a corresponding voltage drive (low source impedance) that is applied directly to network 20. This is tantamount to a collapsing of the column pairs in the FIG. 4 illustration, which leads to the drawing of FIG. 6. Thus, FIG. 6 includes a K-flop neural network 30 and an input interconnection network 50 having one output port of K leads which applies signals to network 30, one input port of K leads which receives signals from network 30, and one input/output port of N leads which serves as an interface to the FIG. 6 network. As in FIG. 1, K is the number of stored vectors and N is the number of bits per vector. In accordance with the above, each output E_j of network 30 contributes with a current drive to the i^{th} amplifier 31 via a connection

$$D_{ij} = \mathrm{EXNOR}(\mathrm{AND}(E_i, M_{ij}), M_{ij}).$$

One embodiment of this logical interconnection arrangement is depicted in the blow-up portion of FIG. 6.

FIG. 7 presents an interesting application of my neural network.

Often it is desirable to perform a cross-correlation computation (or an auto-correlation computation) on an incoming signal. A cross-correlation can be performed, for example, by sampling the signal against which the cross-correlation of an input signal is to be evaluated, to develop a vector M (comprising N bits) and storing vector M as one of the vectors in networks 20 and 40. Shifted replicas of M are then stored as the other vectors of networks 20 and 40. This arrangement is shown in FIG. 7, wherein register 60 is loaded with a reference signal M and the different components of M are loaded into the various cells 22 of FIG. 7 in a staggered fashion to effect the aforedescribed storing of delayed replicas of M. This is shown diagrammatically in FIG. 7 by dashed lines 51,

52 and 53. In operation, an input signal is applied at the input/output port of the FIG. 7 network, yielding shortly thereafter an output vector at the input/output port that is closest to the applied signal. The input and output ports of network 30 give a different and, perhaps, a more useful indication in a correlator application. The output port of network 30 delivers a vector with one component being high, or "1", and the other components being low. The component that is high identifies the particular delayed replica of M that best correlates with the input signal. The input port to network 30 provides the actual correlation values.

Although a number of embodiments have been disclosed herein, still different embodiments and applications will, no doubt, suggest themselves to those who are skilled in art to which this invention pertains.

For example, the above descriptions do not specifically state that the voltages developed by amplifiers 11 and 31 can be any alterable analog values, but such a realization falls squarely within the invention.

In still another example, the concept of using an output other than the output of projection network 20 (in FIG. 1) may be expanded. To illustrate, the output signals of network 30 are as indicative of the selected memory as are the outputs of network 20 and the drive signals of network 40. When network 30 is a K-flop, the output of network 30 is very simple (a "1" in the p^{th} output lead means that the p^{th} vector was selected) and that output can be employed, in encoded or in unencoded form, as the output of the network. Thus, the output of the FIG. 1 network can be derived as shown in FIG. 8, by encoding the outputs of network 30 with encoder 70, loading the encoded output into shift register 80 and extracting the output signals of the FIG. 8 network from the serial output of register 80. This, of course, reduces the number of leads required to interface with the FIG. 8 network. A network 30 that is other than the K-flop can, perhaps, do even without encoder 70.

Also shown in FIG. 8 is a network 40 which employs the drive signals to network 10, plus some additional output leads from an auxiliary network 41, as the output signals of the FIG. 8 network. This permits the FIG. 8 network to operate more than just a content addressable memory which outputs the closest replica of its input. The additional outputs from network 41 can provide whatever additional information it is desired to be stored for each vector. Network 41 is driven by the output signals of network 30.

Claims

1. An associative network for storing K vectors M_i, where i is an index in the range 1 to K and designates a particular vector, and each vector M_i has components M_{ij} where j is an index in the range 1 to N and designates the component number of the vector, K and N being integers, comprising:

    a decision network (30) for developing at K output ports (E_i) of said decision network signals that indicate recognition of a degree of presence of said vectors within input signals appearing at K input ports of said decision network; and

    an interconnection network (40, 10, 20) having K input leads connected to said K output ports and K output leads connected to said K input ports, and N network interface leads (12), where each of said network interface leads, j, is coupled to each output lead, i, of said interconnection network through a connection C_{kj} and to each input lead, k, of said interconnection network through a connection C'_{kj},

    C_{ij} being defined as a logic function of V_j and M_{ij}, where V_j is a signal on a j^{th} lead of said network interface leads (12), and C'_{kj} being defined as a logic function of E_k and M_{kj}, where E_k is a k^{th} output of said decision network (30).

2. A network as claimed in claim 1 wherein said C_{ij} connections develop signals at said K input ports of said decision network (30) that are related to the projections of signals on said network interface leads (12) on said K vectors.

3. A network as claimed in claim 1 wherein each set of said C_{ij} connections for a selected value of j develop a signal at a j^{th} output lead of said interconnection network (40, 10, 20) that is related to the projection of signals on said network interface leads (12) on one of said K vectors.

4. A network as claimed in claim 1 where said C'_{ij} connections develop signals for driving said interconnection network (40, 10, 20) to a state where signals on said network interface leads correspond to one of said K vectors.

5. A network as claimed in claim 1 wherein said decision network (30) is a K-flop network and each set of said C'_i connections for a given subscript j is related to one of said K vectors.

6. A network as claimed in claim 5 wherein each set of said C_{ij} connections develops signals at said K input ports of said K-flop network (30) that are related to the projections of said signals at said network interface leads (12) on said K vectors.

7. A network as claimed in claim 5 wherein each vector M_i of said K vectors comprises bits M_{ij}, and each of said C'_{ij} forms an excitatory connection when M_{ij} = 1 and an inhibitory connection when M_{ij} = 0.

8. A network as claimed in claim 5 wherein each

vector M_j of said K vectors comprises bits M_{ij} and wherein C_{ij} = AND(V_j,M_{ij}), where V_j is a signal on a j^{th} lead of said network interface leads (12).

9. A network as claimed in claim 5 wherein each vector M_j of said K vectors comprises bit M_{ij} and wherein C_{ij} = EXNOR(V_j,M_{ij}), where V_j is a signal on a J^{th} lead of said network interface leads (12).

10. A network as claimed in claim 5 wherein each vector M_j of said K vectors comprises bits M_{ij}, and where C'_{ij} = AND (E_j,M_{ij}), where E_j is a j^{th} output of said K-flop network (30).

11. A network as claimed in claim 5 comprising amplifiers interposed between said interconnection network N input leads and said interconnection network (40, 10, 20) N vector output leads.

12. A network as claimed in claim 1 comprising control means (control 33) connected to said decision network (30) for disabling all output signals at said K output ports.

13. A network as claimed in claim 1, adapted to develop output signals responsive to signals appearing at said K output ports of said decision network (30).

14. A network as claimed in claim 1 comprising a network output port and shift register means (60) interposed between said network output port and said K output ports of said decision network (30).

15. A network as claimed in claim 1 comprising a network output port and decoder means (70) interposed between said network output port and said K output ports of said decision network (30).

16. A network as claimed in claim 1 comprising an auxiliary network (41), responsive to said K output ports of said decision network, for developing signals for additional output leads of said network.

Patentansprüche

1. Assoziatives Netzwerk zur Speicherung von K Vektoren M_i, wobei i ein Index im Bereich zwischen 1 bis K ist und einen bestimmten Vektor bezeichnet, jeder Vektor M_i Komponenten M_{ij} besitzt, j ein Index im Bereich von 1 bis N ist und die Komponentennummer des Vektors bezeichnet und K und N ganze Zahlen sind, mit:
einem Entscheidungsnetzwerk (30) zur Erzeugung an K Ausgangsports (E_i) des Entscheidungsnetzwerks Signale, die die Erkennung eines Wahrscheinlichkeitsgrades für das Vorhandensein der Vektoren in Eingangssignalen anzeigen, welche an K Eingangsports des Entscheidungsnetzwerks erscheinen, und
einem Verbindungsnetzwerk (40,10,20) mit K, mit den K Ausgangsports verbundenen Eingangsleitungen, K, mit den K Eingangsports verbundenen Ausgangsleitungen und N Netzwerk-Schnittstellenleitungen (12), wobei jede Netzwerk-Schnittstellenleitung j mit jeder Ausgangsleitung i des Verbindungsnetzwerks über eine Verbindung C_{kj} und jeder Eingangsleitung k des Verbindungsnetzwerks über eine Verbindung C'_{kj} verbunden ist,
wobei C_{ij} als logische Funktion von V_j und M_{ij} definiert ist, V_j ein Signal auf einer j-ten Leitung der Netzwerk-Schnittstellenleitungen (12) ist, und C'_{kj} als logische Funktion von E_k und M_{kj} definiert ist, und E_k der k-te Ausgang des Entscheidungsnetzwerks (30) ist.

2. Netzwerk nach Anspruch 1, bei dem C_{ij} Verbindungen Signale an den K Eingangsports des Entscheidungsnetzwerks (30) erzeugen, die zu den Projektionen von Signalen auf den Netzwerk-Schnittstellenleitungen (12) auf die K Vektoren in Beziehung stehen.

3. Netzwerk nach Anspruch 1, bei dem jeder Satz von C_{ij} Verbindungen für einen gewählten Wert von j ein Signal auf einer i-ten Ausgangsleitung des Verbindungsnetzwerks (40,10,20) erzeugt, das zu der Projektion von Signalen auf den Netzwerk-Schnittstellenleitungen (12) auf einen der K Vektoren in Beziehung steht.

4. Netzwerk nach Anspruch 1, bei dem die C'_{ij} Verbindungen Signale erzeugen, die das Verbindungsnetzwerk (40,10,20) in einen Zustand treiben, in welchem Signale auf den Netzwerk-Schnittstellenleitungen einem der K Vektoren entsprechen.

5. Netzwerk nach Anspruch 1, bei dem das Entscheidungsnetzwerk (30) ein K-Flop-Netzwerk ist und jeder Satz der C'_i Verbindungen für einen gegebenen Index j in Beziehung zu einem der K Vektoren steht.

6. Netzwerk nach Anspruch 5, bei dem jeder Satz der C_{ij} Verbindungen Signale auf den K Eingangsports des K-Flop-Netzwerks (30) erzeugt, die zu den Projektionen der Signale an den Netzwerk-Schnittstellenleitungen (12) auf die K Vektoren in Beziehung stehen.

7. Netzwerk nach Anspruch 5, bei dem jeder Vektor M_j der K Vektoren Bits M_{ij} umfaßt und jede der C'_{ij}

Verbindungen eine Erregungsverbindung bildet, wenn $M_{ij} = 1$ ist eine Sperrverbindung, wenn $M_{ij} = 0$ ist.

8. Netzwerk nach Anspruch 5, bei dem jeder Vektor M_i der K Vektoren Bits M_{ij} umfaßt und C'_{ij} = UND (V_j, M_{ij}) ist, wobei V_j ein Signal auf einer j-ten Leitung der Netzwerk-Schnittstellenleitungen (12) ist.

9. Netzwerk nach Anspruch 5, bei dem jeder Vektor M_i der K Vektoren Bits M_{ij} umfaßt und C_{ij} = EXNOR (V_j, M_{ij}) ist, wobei V_j ein Signal auf einer j-ten Leitung der Netzwerk-Schnittstellenleitungen (12) ist.

10. Netzwerk nach Anspruch 5, wobei jeder Vektor M_i der K Vektoren Bits M_{ij} umfaßt und C'_{ij} = UND (E_i, M_{ij}) ist, wobei E_i ein j-ter Ausgang des K-Flop-Netzwerks (30).

11. Netzwerk nach Anspruch 5, mit Verstärkern, die zwischen die N Eingangsleitungen des Verbindungsnetzwerks und die N Vektorausgangsleitungen des Verbindungsnetzwerks (40,10,20) geschaltet sind.

12. Netzwerk nach Anspruch 1, mit einer Steuereinrichtung (Steuerung 33), die mit dem Entscheidungsnetzwerk (30) verbunden ist, um alle Ausgangssignale an den K Ausgangsports abzuschalten.

13. Netzwerk nach Anspruch 1, das Ausgangssignale unter Ansprechen auf Signale erzeugt, die an den K Ausgangsports des Entscheidungsnetzwerks (30) erscheinen.

14. Netzwerk nach Anspruch 1, mit einer Netzwerkausgangsport- und Schieberegistereinrichtung (60), die zwischen die Netzwerk-Ausgangsports und die K Ausgangsports des Entscheidungsnetzwerks (30) eingefügt ist.

15. Netzwerk nach Anspruch 1, mit einer Netzwerkausgangsport- und Decodiereinrichtung (70), die zwischen die Netzwerkausgangsports und die K Ausgangsports des Entscheidungsnetzwerks (30) eingefügt ist.

16. Netzwerk nach Anspruch 1, mit einem Hilfsnetzwerk (41), das unter Ansprechen auf die K Ausgangsports des Entscheidungsnetzwerks Signale für zusätzliche Ausgangsleitungen des Netzwerks erzeugt.

Revendications

1. Un réseau associatif pour enregistrer K vecteurs M_i, dans lesquels i est un index dans la plage de 1 à K et désigne un vecteur particulier, et chaque vecteur M_i a des composantes M_{ij} dans lesquelles j est un index dans la plage de 1 à N et désigne le numéro de composante du vecteur, K et N étant des nombres entiers, comprenant :

un réseau de décision (30) pour produire sur K accès de sortie (E_i) de ce réseau de décision des signaux qui indiquent la reconnaissance d'un degré de présence des vecteurs précités dans des signaux d'entrée apparaissant sur K accès d'entrée du réseau de décision; et

un réseau d'interconnexion (40, 10, 20) ayant K conducteurs d'entrée connectés aux K accès de sortie et K conducteurs de sortie connectés aux K accès d'entrée, et N conducteurs d'interface de réseau (12), chacun de ces conducteurs d'interface de réseau, j, étant connecté à chaque conducteur de sortle, i, du réseau d'interconnexion par l'intermédiaire d'une connexion C_{kj} et à chaque conducteur d'entrée, k, du réseau d'interconnexion par l'intermédiaire d'une connexion C'_{kj},

C_{ij} étant définie comme une fonction logique de V_j et M_{ij}, en désignant par V_j un signal sur un j-ième conducteur parmi les conducteurs d'interface de réseau (12), et C'_{kj} étant définie comme une fonction logique de E_k et M_{kj}, en désignant par E_k une k-ième sortie du réseau de décision (30).

2. Un réseau selon la revendication 1, dans lequel les connexions C_{ij} produisent sur les K accès d'entrée du réseau de décision (30) des signaux qui sont liés aux projections, sur les K vecteurs, de signaux présents sur les conducteurs d'interface de réseau (12).

3. Un réseau selon la revendication 1, dans lequel chaque ensemble des connexions C_{ij} pour une valeur sélectionnée de j produit un signal sur un i-ième conducteur de sortie du réseau d'interconnexion (40, 10, 20) qui est lié à la projection, sur l'un des K vecteurs, de signaux présents sur les conducteurs d'interface de réseau (12).

4. Un réseau selon la revendication 1, dans lequel les connexions C'_{ij} produisent des signaux pour attaquer le réseau d'interconnexion (40, 10, 20), pour le faire passer dans un état dans lequel des signaux présents sur les conducteurs d'interface de réseau correspondent à l'un des K vecteurs.

5. Un réseau selon la revendication 1, dans lequel le réseau de décision (30) est un réseau de bas-

cule d'ordre K, et chaque ensemble de connexions C'_i pour un indice j donné est lié à l'un des K vecteurs.

6. Un réseau selon la revendication 5, dans lequel chaque ensemble de connexions C_{ij} produit des signaux sur les K accès d'entrée du réseau de bascule d'ordre K (30) qui sont liés aux projections, sur les K vecteurs, des signaux présents sur les conducteurs d'interface de réseau (12).

7. Un réseau selon la revendication 5, dans lequel chaque vecteur M_j parmi les K vecteurs comprend des bits M_{ij}, et chacune des C'_{ij} forme une connexion d'excitation lorsque $M_{ij} = 1$ et une connexion d'inhibition lorsque $M_{ij} = 0$.

8. Un réseau selon la revendication 5, dans lequel chaque vecteur M_j parmi les K vecteurs comprend des bits M_{ij}, et dans lequel C_{ij} = ET(V_j,M_{ij}), en désignant par V_j un signal sur un j-ième conducteur parmi les conducteurs d'interface de réseau (12).

9. Un réseau selon la revendication 5, dans lequel chaque vecteur M_j parmi les K vecteurs comprend des bits M_{ij}, et dans lequel C_{ij} = NON-OU-EX(V_j,M_{ij}), en désignant par V_j un signal sur un j-ième conducteur parmi les conducteurs d'interface de réseau (12).

10. Un réseau selon la revendication 5, dans lequel chaque vecteur M_j parmi les K vecteurs comprend des bits M_{ij}, et dans lequel C'_{ij} = ET(E_j,M_{ij}), en désignant par E_j une j-ième sortie du réseau de bascule d'ordre K (30).

11. Un réseau selon la revendication 5, comprenant des amplificateurs interposés entre les N conducteurs d'entrée du réseau d'interconnexion et les N conducteurs de sortie de vecteur du réseau d'interconnexion (40, 10, 20).

12. Un réseau selon la revendication 1, comprenant des moyens de commande (conducteur de commande 33) connectés au réseau de décision (30) pour invalider tous les signaux de sortie sur les K accès de sortie.

13. Un réseau selon la revendication 1, conçu pour produire des signaux de sortie sous la dépendance de signaux qui apparaissent sur K accès de sortie du réseau de décision (30).

14. Un réseau selon la revendication 1, comprenant un accès de sortie de réseau et une structure de registre à décalage (60) intercalée entre cet accès de sortie de réseau et K accès de sortie du réseau de décision (30).

15. Un réseau selon la revendication 1, comprenant un accès de sortie de réseau et des moyens décodeurs (70) intercalés entre cet accès de sortie de réseau et K accès de sortie du réseau de décision (30).

16. Un réseau selon la revendication 1, comprenant un réseau auxiliaire (41), fonctionnant sous la dépendance des K accès de sortie du réseau de décision, pour produire des signaux pour des conducteurs de sortie supplémentaires du réseau.

FIG. 1

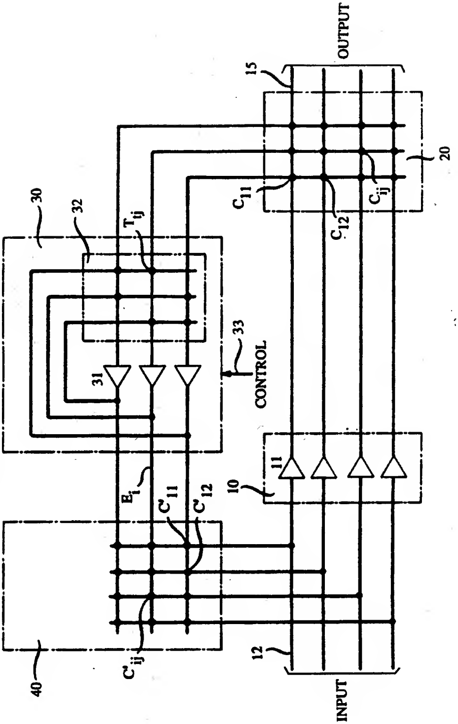

OUTPUT
15
20
C_{11}
C_{12}
C_{ij}
30
32
T_{ij}
33
CONTROL
31
11
10
E_i
C'_{11}
C'_{12}
C'_{ij}
40
12
INPUT

FIG. 2

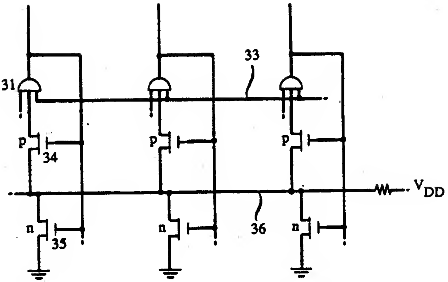


FIG. 3

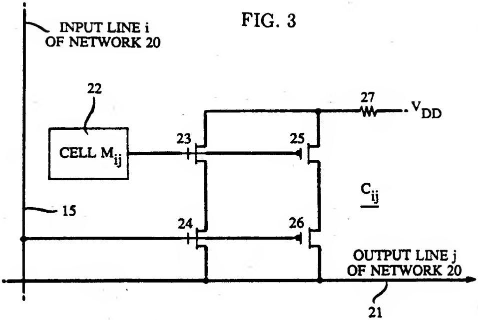
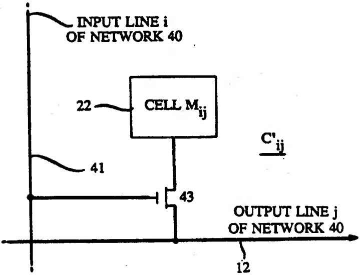

INPUT LINE i
OF NETWORK 20
22
CELL M_{ij}
23
25
27
V_{DD}
C_{ij}
15
24
26
OUTPUT LINE j
OF NETWORK 20
21

FIG. 4


INPUT LINE i
OF NETWORK 40
22
CELL M_{ij}
C'_{ij}
41
43
OUTPUT LINE j
OF NETWORK 40
12

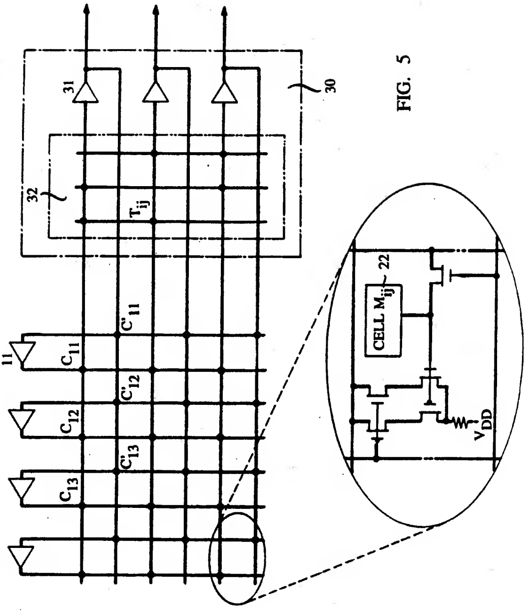


FIG. 5

FIG. 6

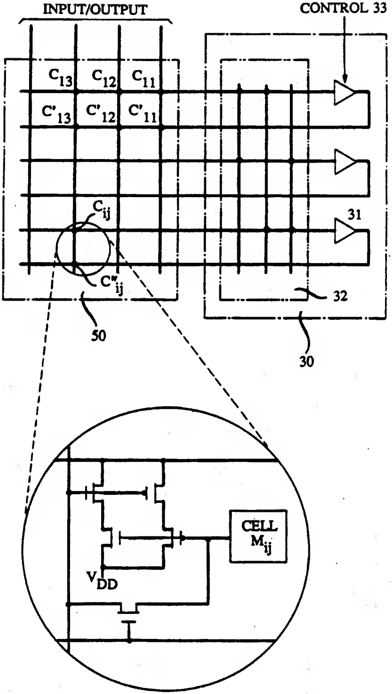
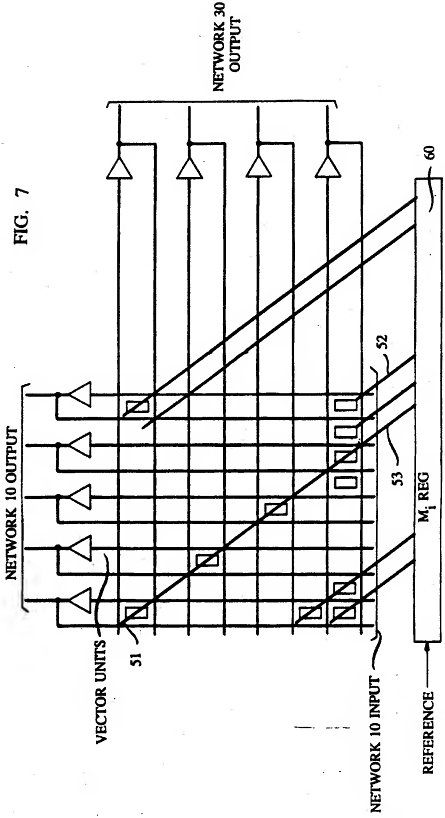

INPUT/OUTPUT
CONTROL 33
C13
C12
C11
C'13
C'12
C'11
Cij
C"ij
31
32
50
30
CELL
Mij
VDD

FIG. 7


NETWORK 30
OUTPUT
NETWORK 10 OUTPUT
VECTOR UNITS
51
52
53
60
M_i REG
NETWORK 10 INPUT
REFERENCE

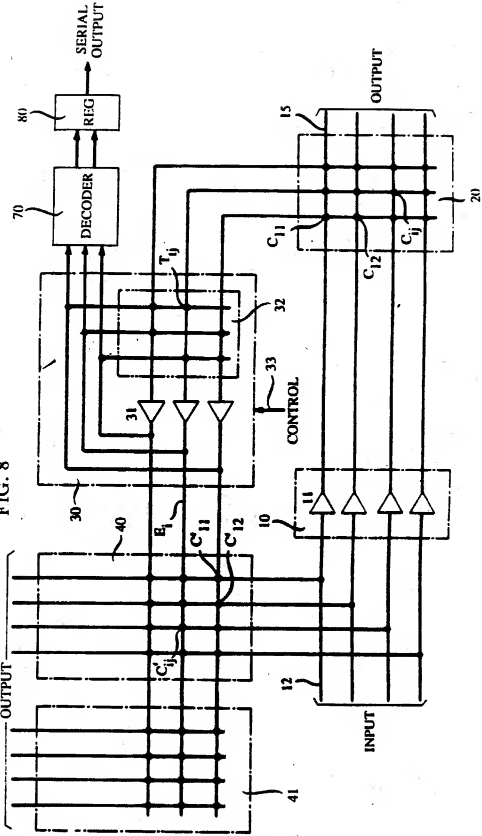

SERIAL OUTPUT
REG
80
DECODER
70
OUTPUT
15
20
C11
C12
Cij
Tij
32
33
CONTROL
31
30
40
Ei
C'11
C'12
10
11
C'ij
12
INPUT
OUTPUT
41

FIG. 8